What is claimed is:

1. A method of using a branch target buffer having a plurality of banks, comprising:

receiving an Instruction Pointer (IP) signal, the instruction pointer signal comprising an IP tag field and an IP set field;

reading a plurality of entries corresponding to the IP set field, each of the entries comprising an entry tag, an entry bank, and entry data; and

comparing (i) each entry tag and entry bank with (ii) the IP tag and each of the plurality of banks.

2. The method of claim 1, further comprising selecting data based on results of said comparing.

3. The method of claim 1, wherein said comparing concatenates (i) each entry tag and entry bank and (ii) the IP tag and a number representing each of the plurality of banks.

4. The method of claim 2, wherein each entry further comprises an entry valid field and said selecting is further based on the entry valid field.

5. The method of claim 1, wherein the plurality of banks in the branch target buffer are implemented in a single array.

6. The method of claim 1, wherein each entry further comprises an entry valid field and different entries do not have identical entry tag, entry bank and entry valid values.

7. The method of claim 1, further comprising decoding the IP set field.

8. The method of claim 2, wherein said selecting selects data providing branch information related to a cache line that is being read.

9. The method of claim 1, wherein each of the plurality of banks is organized in a set associative fashion.

10. A banked branch target buffer, comprising:

an input port configured to receive a look-up Instruction Pointer (IP) comprising an IP tag field and an IP set field, the IP set field identifying a plurality of information entries comprising an entry tag, an entry bank and entry data; and

a comparator coupled to said input port and configured to compare (i) the IP tag and a bank identifier with (ii) the entry tag and entry bank of each information entry.

11. The banked branch target buffer of claim 10, wherein said comparator compares (i) each entry tag concatenated with the entry bank for that entry and (ii) the IP tag concatenated with a number representing each of the plurality of banks.

12. The banked branch target buffer of claim 10, wherein each entry further comprises an entry valid field and data is select based on the entry valid field.

13. The banked branch target buffer of claim 10, wherein the branch target buffer has a plurality of banks implemented in a single array.

14. The banked branch target buffer of claim 13, wherein each of the plurality of banks is organized in a set associative fashion.

15. The banked branch target buffer of claim 10, wherein each entry further comprises an entry valid field and different entries do not have identical entry tag, entry bank and entry valid values.

16. The banked branch target buffer of claim 10, wherein the IP set field is decoded and used to read out the entries.

17. The banked branch target buffer of claim 10, wherein data is selected to provide branch information related to a cache line that is being read.

18. In a computer processor coupled to a memory, said memory divided into memory blocks, a branch prediction mechanism, said branch prediction mechanism predicting a block of memory to fetch based upon an instruction pointer that points to a currently executing instruction, said branch instruction prediction mechanism comprising:

a branch target buffer cache comprising a plurality of ordered branch target buffer banks formed as a single array, each said ordered branch target buffer bank comprising a plurality of

branch entries storing information about branch instructions addressed by address bits specifying a different subblock within said memory blocks;

a branch prediction circuit, said branch prediction circuit receiving said instruction pointer, said branch prediction circuit indexing into all of said ordered branch target buffer banks of said branch target buffer cache circuit fetching at most one branch entry from each said plurality of branch target buffer banks; and

a prioritizer circuit, said prioritizer circuit indicating the selection of one of said branch entries fetched by said branch prediction circuit from said ordered branch target buffer banks by selecting a first taken branch instruction located after said instruction pointer.

19. In a computer system, a method of predicting a block of memory to fetch based upon an instruction pointer that points to a currently executing instruction, said method comprising:

receiving a current instruction pointer in a branch prediction mechanism, said branch prediction mechanism comprising a plurality of ordered branch target buffer banks formed as a single array;

indexing into all of said plurality of ordered branch target buffer banks, each said branch target buffer bank comprising a plurality of branch entries storing information about branch instructions addressed by address bits specifying a different subblock within said memory blocks;

retrieving at most one ordered branch entry from each said ordered branch target buffer banks; and

selecting a next upcoming branch instruction from said retrieved ordered branch entries.